FORESEE®

tSD (G3A) Specification (3.3V)

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Reversion History:

Rev.	Date	Changes	Remark
A0	2013/01/02	Basic spec and architecture	
A1	2013/07/11	Updated a new product type	
A2	2013/08/08	Updated a new product type	Preliminary

CONTENTS

1. Introduction

FORESEE tSD (TSOP SD) is an SD Card designed in a TSOP package form, whose pin-out are the same as TSOP NAND flash. The “NC” pin of NAND flash is designed for SD card interface, and tSD design is completely compatible with NAND flash layout. The tSD controller can manage wear leveling, bad block management and provide higher ECC, and the host system can support the new process flash without updating its hardware or software, which is very important as the NAND flash becomes increasingly complies with current advanced NAND process. Host system will be able to access tSD device of new flash technology without updating their host hardware or software. (The host system is required to support SD Card booting function). FORESEE tSD is designed to cover a wide area of applications, such as DTV, IPTV, GPS, PND, Tablet PC, MP4 players, E-Learning machine, electronic toys, etc. Targeted features are high mobility and high performance at a competitive cost.

FORESEE tSD is compatible with SD ver.2.0 and Ver.1.1 specifications, offering high performance, high quality and low power consumption. FORESEE tSD provides capacities from 4GB to 32GB.

2. Product List

Product ID	Capacity	Package
NCTSTS86-04G	3.60GB	12x20x1.2(mm)
NCTSTS76-08G	7.20GB	12x20x1.2(mm)
NCTSTS76-16G	14.4GB	12x20x1.2(mm)

3. Features

- Supports SD specifications v1.01/v1.1/v2.0
- Compatible with products requiring an SD interface and Flash storage
- Higher IOPS for embedded application by enabling the enhanced NAND Flash area
- 4-bit data bus with max 50MHz bus clock rate
- Supports SPI Mode
- Hardware ECC engine
- Unique firmware backup mechanism
- Global wear leveling to expend NAND flash lifetime
- Power-loss safeguard
- Powerful L2P NAND flash management algorithm
- IDA (Initial Data Accelerating)

4. tSD Function Description

FORESEE tSD contains an intelligent subsystem which provides useful capabilities:

- Host independence from details of operating NAND flash.
- Internal ECC to correct defect in NAND flash.
- Automatic sleep mode for conserving power.

Comparing with normal SD card, FORESEE tSD provides extra amazing functions without applying any modifications to the host. , Which consist of:

- Unique firmware backup mechanism

There are several firmware copies in this memory card. Each one can be used for the card to boot. Normally, the card can boot with the first firmware copy. In some extreme cases, it can also boot with the other three copies. This mechanism enhances its stability.

- Global wear leveling

To achieve the best stability and device life time, this card has its own global wear leveling algorithm. It ensures that not only normal area, but also the frequently accessed area, such as FAT, is wrote and erased evenly.

- Power-loss safeguard

To prevent from false operating, a mechanism named power-loss safeguard is applied in the memory card. In the case of sudden power-loss, the memory card can still work normally when it gets power again.

- IDA(Initial Data Accelerating)

IDA may accelerate the Initial data written to the tSD, saving the time up to 50% off in the downloading process.

5. Product Specifications

5.1 Read/Write Performance (Typical value)

Product ID	Sequential Write	Sequential Read
NCTSTS86-04G	6MB/S	12MB/S
NCTSTS76-08G	6MB/S	12MB/S
NCTSTS76-16G	6MB/S	14MB/S

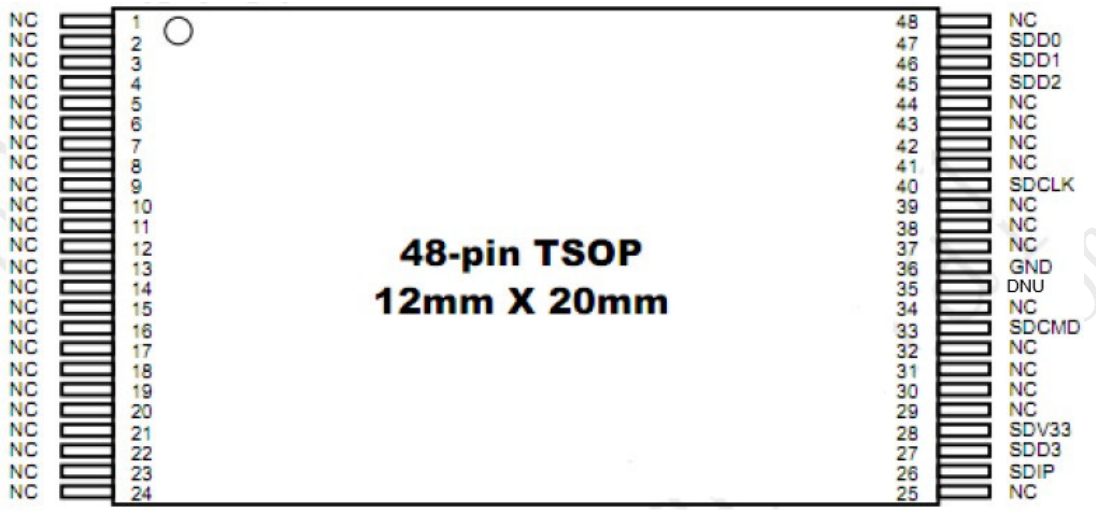
5.2 Power Consumption

Product ID	Status	Max Value	Average Value
NCTSTS86-04G	Standby current	250uA	60uA
	Operating current	100mA	50mA
NCTSTS76-08G	Standby current	250uA	75uA
	Operating current	100mA	50mA
NCTSTS76-16G	Standby current	250uA	75uA
	Operating current	100mA	50mA

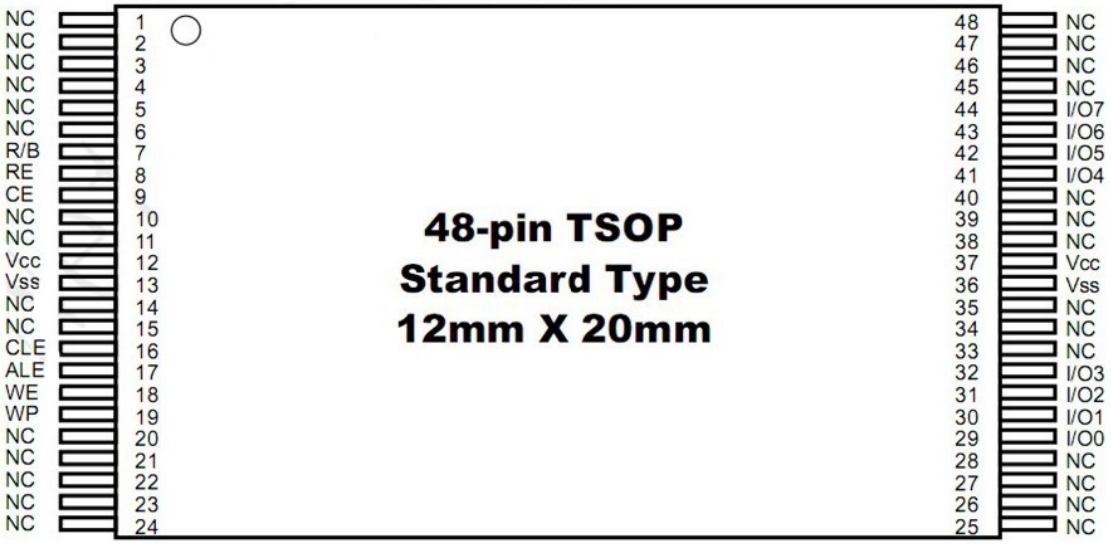
5.3 Operational Environment

Mode	Temperature
Operating	-25° C to 85° C
Storage without operation	-45° C to 85° C

6. Pin Assignment



FORESEE tSD outline



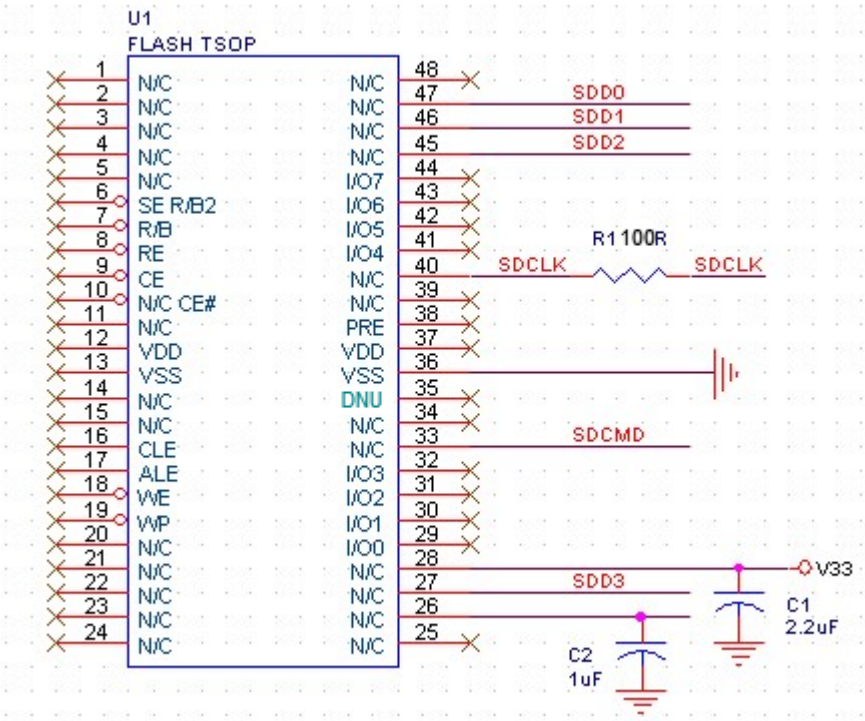
TSOP48 NAND Flash outline

Pin No.	SD Mode		
	Name	Type	Description
26	SDIP	S	SD Internal Power. This pin is neither output nor input.
27	SDD3	I/O/PP	SD Data Line [Bit 3]
28	SDV33	S	SD Power 3.3v Supply
33	SDCMD	PP	Command/Response
35	DNU	DNU	Do Not Use
36	GND	S	Supply voltage ground
40	CLK	I	Clock
45	SDD2	I/O/PP	SD Data Line [Bit 2]
46	SDD1	I/O/PP	SD Data Line [Bit 1]
47	SDD0	I/O/PP	SD Data Line [Bit 0]

S: power supply; I: input; O: output; PP: I/O using push-pull drivers

6.1 An Example

Here is an example of hardware connection diagram. It is just for reference and the schematic can be changed depending on the environment of the system.

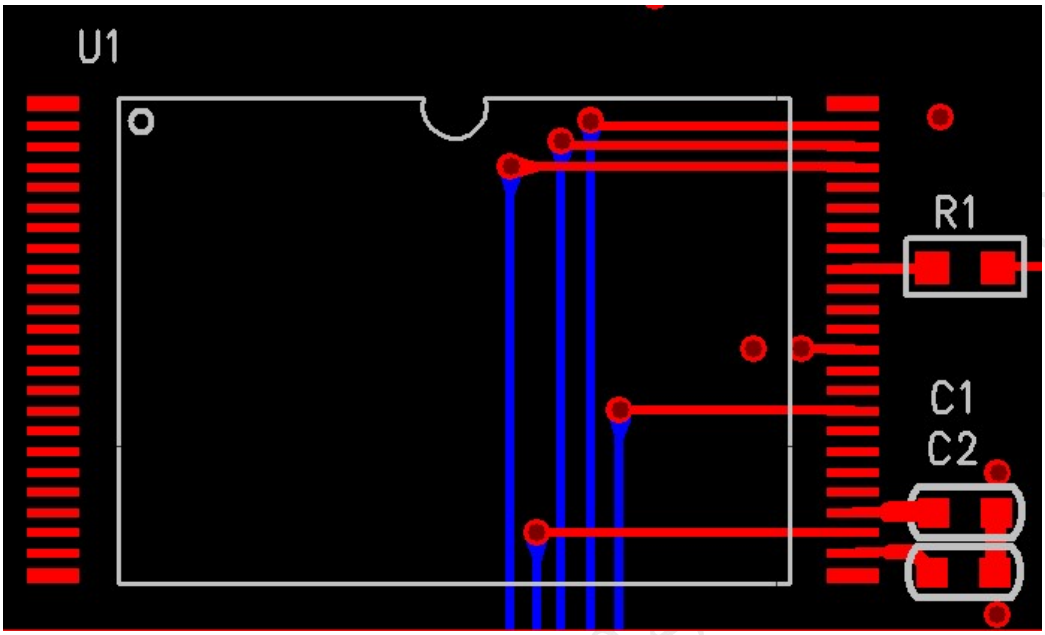


Note:

1 . Ceramic capacitors (1uF or 2.2uF) are required between pin26 (SDIP) and SDGND, and between pin28 (SDV33) and SDGND. And it would be necessary to connect a resistor (33Ω/68 Ω/100Ω, and 68Ω is default) in series with pin40 (SDCLK).

2 . Pin 35 is not supposed to be used.

You can also make a co-layout of FORESEE tSD (TSOP, SD2.0), eMMC (BGA) and FORESEE fSD (BGA, SD2.0), as below.



7. Usage overview

7.1 Commands Introduction

Host accesses tSD by issuing a collection of commands. There are four kinds of commands defined to control the SD Memory Card:

- Broadcast commands (BC), no response - The broadcast feature is only if all the CMD lines are connected together in the host. If they are separated, then each card will accept it separately in its turn.
- Broadcast commands with response (BCR)
  response from all cards simultaneously - Since there is no Open Drain mode in SD Memory Card, this type of command shall be used only if all the CMD lines are separated - the command will be accepted and responded by every card separately.
- Addressed (point-to-point) commands (AC)
  No data transfer on DAT
- Addressed (point-to-point) data transfer commands (ADTC)
  Data transfer on DAT

All commands and responses are sent over the CMD line of the SD Memory Card. The command transmission always starts with the left bit of the bit string corresponding to the command codeword.

All commands have a fixed code length of 48 bits, needing a transmission time of 1.92μs @ 25 MHz and 0.96μs @ 50MHz.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	x	x	x	'1'
Description	start bit	transmission bit	CMD index	Argument	CRC7	end bit

A command always starts with a start bit (always 0), followed by the bit indicating the direction of transmission (host = 1). The next 6 bits indicate the index of the command, this value being interpreted as a binary coded number (between 0 and 63). Some commands need an argument (e.g. an address), which is coded by 32 bits. A value denoted by 'x' in the table above indicates this variable is dependent on the command. All commands are protected by a CRC. Every command codeword is terminated by the end bit (always 1).

The command set of the tSD Memory Card system is divided into several classes. Each class supports a set of card functionalities.

A CCC (Card Command Class) bit, which corresponds to a supported command number, is set to 1. A class in CCC includes mandatory commands is always set to 1. Cards with specific functions may need to support some optional commands. For example, Combo Card shall support CMD5.

7.2 Responses

All responses are sent via the command line CMD. The response transmission always starts with the left bit of the bit string corresponding to the response codeword. The code length depends on the response type.

A response always starts with a start bit (always 0), followed by the bit indicating the direction of transmission (card = 0). All responses except for the type R3 are protected by a CRC. Every command codeword is terminated by the end bit (always 1).

There are five types of responses for the SD Memory Card. The SDIO Card supports additional response types named R4 and R5. Refer to SDIO Card Spec for detailed information on the SDIO commands and responses.

7.3 Memory Array Partitioning

The basic unit of data transfer to/from the SD Memory Card is one byte. All data transfer operations that require a block size always define block lengths as integer multiples of bytes. Some special functions need other partition granularity.

For block-oriented commands, the following definition is used:

- Block: is the unit that is related to the block oriented read and write commands. Its size is the number of bytes that will be transferred when one block command is sent by the host. The size of a block is either programmable or fixed. The information about allowed block sizes and the programmability is stored in the CSD.

For devices that have erasable memory cells, special erase commands are defined. The granularity of the erasable units is in general not the same as for the block oriented commands:

- Sector: is the unit that is related to the erase commands. Its size is the number of blocks that will be erased in one portion. The size of a sector is fixed for each device. The information about the sector size (in blocks) is stored in the CSD. Note that if the card specifies AU size, sector size should be ignored.
- AU (Allocation Unit): is a physical boundary of the card and consists of one or more blocks and its size depends on each card. The maximum AU size is defined for memory capacity. Furthermore AU is the minimal unit in which the card guarantees its performance for devices which complies with Speed Class Specification. The information about the size and the Speed Class are stored in the SD Status. AU is also used to calculate the erase timeout.
- WP-Group: is the minimal unit that may have individual write protection for devices which support write-protected group. Its size is the number of groups that will be write-protected by one bit. The size of a WP-group is fixed for each device. The information about the size is stored in the CSD. The High Capacity SD Memory Card does not support the write protect group command.

Each WP-group may have an additional write protection bit. The write protection bits are programmable via special commands.

Both functions are optional and only useful for writable/erasable devices. The write protection may also be useful for multi type cards (e.g. a ROM - Flash combination). The information about the availability is stored in the CSD.

(For more details, please refer to SDA Physical Layer Specification, Version 2.00)

8. SD Register Table

The following table shows the register list for current specifications. For detailed functionality, please refer to the latest SD specifications.

Register Name	SD 2.0	SD 1.1	SD 1.01
Operation Condition Register (OCR)	V	V	V
Card Identification Register (CID)	V	V	V
Driver Stage Register (DSR)	NA	NA	NA
Relative Card Address Register (RCA)	V	V	V
Card Specific Data Register (CSD)	V	V	V
SD card Configuration Register (SCR)	V	V	V

8.1. Operation Condition Register (OCR)

The 32-bit operation condition register stores the VDD voltage profile of the card. Additionally,

this register includes status information bits. One status bit is set when the card power-up procedure is finished. This register includes another status bit indicating card capacity status after the power-up status bit is set. The OCR register is implemented by all cards. The supported voltage range is coded as shown in the following table. As long as the card is busy, the corresponding bit (31) is set to low signal.

Furthermore, this register includes 2 other status information bits.

Bit 31 – Card power-up status bit is set when the card power-up procedure is complete.

Bit 30 – Card capacity status bit is set to 1 when the card is a high-capacity SD memory card. Notably, 0 indicates that the card is a standard-capacity SD memory card. The card capacity status bit is valid after the card power-up procedure is complete and card power-up status bit is set to 1. The host reads this status bit to determine whether the card is a standard- or high- capacity SD memory card.

OCR Bit	VDD Voltage Window	High Voltage SD
[6:0]	Reserved	000 0000 b
[7]	1.7V – 1.95V	0 b
[14:8]	2.0V – 2.6V	000 0000 b
[23:15]	2.7V – 3.6V	1 1111 1111 b
[29:24]	Reserved	00 0000 b
[30]	Card capacity status	
[31]	Card power up status bit	

Notes:

1. OCR bit [31] is set to LOW if the card has not finished the power up routine.
2. OCR bit [30] is valid only when the card power up status bit is set.

8.2. Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have a unique identification number. The structure of the CID register is defined in the following table:

CID-slice	Width	Name	Field
[127:120]	8	Manufacturer ID	MID
[119:104]	16	OEM/Application ID	OID
[103:64]	40	Product name	PNM
[63:56]	8	Product revision	PRV
[55:24]	32	Product serial number	PSN
[23:20]	4	reserved	-
[19:8]	12	Manufacturing date	MDT
[7:1]	7	CRC7 checksum	CRC
[0:0]	1	not used, always 1	-

8.3. Driver Stage Register (DSR)

The 16-bit driver stage register is optionally utilized to enhance bus performance for extended operating conditions. The CSD register stores information about DSR usage. This register is not

implemented in FORESEE tSD. It is optional.

8.4. Relative Card Address Register (RCA)

The writable 16-bit relative card address register stores the card address. This address is published by the card during card identification, and is used for host-card communication following the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved for setting all cards in the Stand-by State with CMD7.

8.5. CSD Register (CSD Version 2.0)

The following table shows Definition of the CSD Version 2.0 for the High Capacity SD Memory Card and Extended Capacity SD Memory Card. The following sections describe the CSD fields and the relevant data types for the High Capacity SD Memory Card. CSD Version 2.0 are applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0.

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure	D_STRUCTURE	2	01b	R	[127:126]
reserved	-	6	00 0000b	R	[125:120]
data read access-time	(TAAC)	8	0Eh	R	[119:112]
data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
Max. data transfer rate	(TRAN_SPEED)	8	32h or 5Ah	R	[103:96]
card command classes	CCC	12	01x1101 10101b	R	[95:84]
Max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
write block misalignment	(WRITE_BLK_MISALIGN)	1	0	R	[78:78]
read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]
DSR implemented	DSR_IMP	1	x	R	[76:76]
reserved	-	6	00 0000b	R	[75:70]
device size	C_SIZE	22	00 xxxxh	R	[69:48]

reserved	-	1	0	R	[47:47]
erase single block enable	(ERASE_BLK_EN)	1	1	R	[46:46]
erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
write protect group size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
write protect group enable	(WP_GRP_ENABLE)	1	0	R	[31:31]
reserved	-	2	00b	R	[30:29]
write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
Max. write data block length	(WRITE_BL_LEN)	4	9	R	[25:22]
partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	0	R	[21:21]
reserved	-	5	00000b	R	[20:16]
File format group	(FILE_FORMAT_GRP)	1	0	R	[15:15]
copy flag (OTP)	COPY	1	x	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R	[7:1]
not used, always'1'	-	1	1	-	[0:0]

Note: R = readable,
W (1) = writable once,
W = multiple writable

8.6. SD Card Configuration Register (SCR)

The SCR register is another configuration register in a SD card. The SCR stores an SD card's special features, which were configured in a given card. The size of the SCR is 64 bits. SCR is a read only register.

SCR Bit	Width	Name	Field	Value	Note
[63:60]	4	SCR structure	SCR_STRUCTURE	0000 b	v1.0-v2.0
[59:56]	4	SD card spec. version	SD_SPEC	0010 b	
[55]	1	Data status after erase	DATA_STAT_AFTER_ERASE	0 b	

[54:52]	3	SD security support	SD_SECURITY	011 b	
[51:48]	4	DAT bus width support	SD_BUS_WIDTH	0101 b	
[47:32]	16	Reserved	--	--	--
[31:0]	32	Reserved	--	--	--

9. Package Dimensions